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UTILITY PATENT APPLICATION TRANSMITTAL (*Only for new nonprovisional applications under 37 CFR 1.53(b)*)	*Attorney Docket No.* G0631/7010
	First Named Inventor or Application Identifier
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	Express Mail Label No. EL 018 080 843 US
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ■ Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. ■ Specification [Total pages 19]
   13 pages specification
   1 pages abstract
   5 pages claims
   27 claims
3. ■ Drawing(s) *(35 USC 113)* [Total sheets 4]
   ■ Informal I [Total drawings 1-8b]
4. ■ Oath or Declaration [Total pages 2]
   a. ■ Newly executed (fax copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference
   (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & documents(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
   (when there is an assignee)
10. ☐ English Translation of Document *(if applicable)*
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 Γ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ■ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)

16. Other:

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

☐ Cancel in this application original claims of the prior application before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

This application is a ☐ continuation ☐ divisional of application serial no. , filed , entitled , and now .

428706.1

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DATE	January 10, 2000

Attorney Docket No. G0631/7010

Inventor or Identifier: Seamus Paul Whiston and Andrew David Bain

Serial No: Not yet assigned

Filed: Herewith

For: *METHOD FOR FORMING A DMOS DEVICE AND A DMOS DEVICE*

CHECK BOX, if applicable:

☐ **DUPLICATE**

Fee Calculation Sheet

CLAIMS	FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
	TOTAL CLAIMS (37 CFR 1.16(c))	27-20=	7 x	$18	= $126.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	2-3=	0 x	$78	= $0.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d)) +			$	= $0.00
				BASIC FEE (37 CFR 1 16(a))	$ 760.00
			Total of above Calculations =		$886.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1 9, 1.27, 1.28).				$886.00
	Assignment Recordation Fee (if any)				$ 0.00
	Other Fees (e.g., Petition for Extension of Time), if any **NOTE: Enter small-entity amount if applicable.**				$ 0.00
	TOTAL =				$886.00

1. A check in the amount of $886.00 is enclosed.

General Authorization to Charge Deposit Account and General Request for Extension of Time

2. a. ■ If the filing of any paper in this application necessitates the payment of a fee under 37 CFR э ■1.16 ■1.17 or ☐ 1.18, and the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.

   b. ☐ The applicant hereby revokes any prior authorization to charge a fee due under 37 CFR э ☐ 1.16 ☐ 1.17 or ☐ 1.18.

3. If the filing of any paper in this application necessitates an extension of time under 37 CFR э1.136(a), the applicant hereby requests such extension of time. If the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.

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Docket No. G0631/7010
Date: January 10, 2000

"A method for forming a DMOS device and a DMOS device"

Field of the Invention

The present invention relates to a method for forming a DMOS device, and in particular, to a method for forming a body region in a drain region of the DMOS device appropriately aligned in the DMOS device. The invention also relates to a DMOS device.

Background to the Invention

Power integrated circuits in many cases require a combination of lateral DMOS (LDMOS) devices and CMOS devices as well as bipolar CMOS (BiCMOS) devices on the same chip. Indeed, there are many other types of integrated circuits where it is desirable to provide a combination of DMOS and CMOS and/or BiCMOS devices on the same chip. From here on the term "CMOS process" is intended to cover both CMOS and BiCMOS processes. However, known processes for forming DMOS devices are different to known processes for forming CMOS devices, and thus, in general, where it is desired to produce a wafer comprising chips having combinations of DMOS and CMOS devices, the wafer must be subjected to both CMOS and DMOS forming processes. This adds considerably to both the production time and cost of producing such chips with combinations of CMOS and DMOS devices. In the manufacture of DMOS devices, and in particular, LDMOS devices it is essential that a body region which is to be formed in the drain region of the LDMOS device should extend partly beneath the gate of the device, and furthermore, should be appropriately aligned with the gate of LDMOS device.

In a paper entitled "LDMOS Implementation by Large Tilt Implant in 0.6µm BCD5 Process, Flash Memory Compatible" read at the International Symposium of Power Semiconductor Devices, May 1996, and published with the proceedings of the Symposium, Contiero, et al of SGS-Thompson Microelectronics disclose a method for integrating a self-aligned lateral DNMOS (LDNMOS) device into a bipolar CMOS, DMOS process. In this process the LDNMOS device is fabricated up to and including the gate using a CMOS process. The P-body region is then formed beneath the gate by implanting an appropriate dopant into the drain region at an angle to the surface of the drain region using an edge of the gate to form part of the mask on the drain region which defines the area of the surface of the drain region through which the dopant is to be implanted. The dopant is directed in a direction towards the drain region and the edge of the gate for implanting the dopant partly under the gate. In other words, the dopant is implanted using a single large angle of tilt from a perpendicular axis extending from the general plane of a wafer on which the device is being formed. Subsequent to implanting the dopant is diffused into a portion of the drain region for forming the P-body using a suitable CMOS diffusion process. Contiero, et al disclose three possible tilt angles, namely, 30°, 40° and 60°, from which the single tilt angle may be selected. A 45° dopant implant tilt angle appears from the paper of Contiero, et al to be the optimum.

While in the method of Contiero, et al the P-body extends beneath the gate, and is appropriately aligned therewith, the LDNMOS of Contiero, et al suffers from a number of disadvantages. In particular, it is difficult using the method of Contiero, et al to determine the breakdown voltage from source to drain in a lateral or a vertical direction due to punchthrough independently of the drain/source threshold voltage in

the LDMOS for a particular well doping concentration, and vice versa. In order to achieve a desirably low drain/source threshold voltage the dose and energy level of the dopant required are such as to result in a relatively low punchthrough breakdown voltage, while on the other hand if the dopant dosage and energy level is set to achieve a relatively high punchthrough breakdown voltage the drain/source threshold voltage is undesirably high. Similarly it is difficult using the method of Contiero, et al to determine the avalanche breakdown voltage independently of the drain/source threshold voltage in the LDMOS. Thus, while the method proposed by Contiero, et al provides for the forming of an LDNMOS device using a CMOS process, the LDNMOS device, in general, is unsuitable for most applications.

There is therefore a need for a method for producing a DMOS device which overcomes these problems, and in particular, a method for forming such a DMOS device using a CMOS process.

The present invention is directed towards providing such a method and a DMOS device.

<u>**Summary of the Invention**</u>

According to the invention there is provided a method for forming a body region in a drain region of a DMOS device on a wafer after the gate has been formed with the body region extending partly beneath a gate of the DMOS device and appropriately aligned with the gate, the drain region defining a surface plane, the method comprising the steps of:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

Preferably, the dopant is directed at the first angle towards the surface plane in step (a) in a general source/drain direction. Advantageously, the dopant is directed at the second angle towards the surface plane in step (b) in a general source/drain direction.

In one embodiment of the invention the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 30° to 60°. Preferably, the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 40° to 50°. Advantageously, the first angle to the surface plane of the drain region at which the dopant is directed in step (a) is approximately 45°.

In another embodiment of the invention the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 70° to 90°. Preferably, the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 78° to 88°. Advantageously, the second angle to the surface plane of the drain region at which the dopant is directed in step (b) is approximately 83°.

In one embodiment of the invention the dopant is implanted in the drain region in each of steps (a) and (b) using an edge of the gate adjacent the source as part of a mask for defining a portion of the surface of the drain region through which the dopant is to be implanted. The dopant implanted in each of steps (a) and (b) may be the same or different, and the dopant implanted in each of steps (a) and (b) may be implanted at the same or different dose and/or energy levels.

In one embodiment of the invention the dopant implanted in the drain region in each of steps (a) and (b) is diffused by a dopant diffusion process for forming the body region. Alternatively, the dopant implanted in the drain region in each of the steps (a) and (b) is diffused in the drain region before the dopant of the next of the steps (a) and (b) is implanted.

In one embodiment of the invention step (a) is carried out before step (b).

In another embodiment of the invention the drain region is formed by an N-well, and the body region is formed as a P-body, and the dopant of each of steps (a) and (b) is boron.

In a further embodiment of the invention the drain region is formed by a P-well, and the body region is an N-body, and the dopant of each of steps (a) and (b) is phosphorous.

Ideally, the dose and energy levels of the dopant implanted in each of steps (a) and (b) are sufficient for providing the desired drain/source threshold voltage and the breakdown voltage through the drain region.

In one embodiment of the invention the breakdown voltage exceeds the drain/source threshold voltage.

In one embodiment of the invention the method for forming the body region in the drain region of the DMOS device is a CMOS process, and in general, a CMOS device is formed on the wafer by the CMOS process. In another embodiment of the invention the method for forming the body region in the drain region of the DMOS device is a BiCMOS process, and in general, a BiCMOS device is formed on the wafer by the BiCMOS process.

In one embodiment of the invention the DMOS device is an LDMOS device, and may be an LDPMOS and/or an LDNMOS. Additionally, the DMOS may be a vertical DMOS.

Additionally, the invention provides a DMOS device comprising a drain region defining a surface plane, a gate located on the drain region, and a body region

formed in the drain region and extending partly beneath the gate and appropriately aligned therewith, the body region being formed after the gate region has been formed by:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

In one embodiment of the invention the DMOS device is an LDMOS device, and may be an LDNMOS device or a LDPMOS device. Additionally, the DMOS may be a vertical DMOS.

Further the invention provides an integrated circuit chip comprising a DMOS device according to the invention, and the integrated circuit chip may also comprise a CMOS device or a BiCMOS device.

Advantages of the Invention

The advantages of the invention are many. A particularly important advantage of the invention is that it permits LDNMOS and LDPMOS devices to be formed using a conventional CMOS or BiCMOS process, and thus, LDNMOS and LDPMOS devices may be formed simultaneously with the formation of CMOS and/or BiCMOS devices. In particular, by adapting the CMOS process according to the invention the drain/source threshold voltage of the respective LDNMOS and LDPMOS devices can be determined independently of the punchthrough breakdown voltage of the devices, and indeed, independently of the avalanche breakdown voltage. The method according to the invention may be used for forming vertical DMOS devices with similar advantages. Thus, the invention overcomes the problems of forming LDNMOS and LDPMOS devices using CMOS processes known heretofore.

The invention will be more clearly understood from the following description of a preferred embodiment thereof which is given by way of example only with reference to the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a transverse cross-sectional elevational view of an LDNMOS and an LDPMOS according to the invention formed on a silicon substrate by a CMOS process using a method according to the invention,

Fig. 2 is a transverse cross-sectional elevational view of the LDNMOS and the LDPMOS of Fig. 1 in the process of being formed,

Fig. 3 is a view similar to Fig. 2 of the LDNMOS and the LDPMOS at the next stage of their formation after that of Fig. 2,

Fig. 4 is a view similar to Fig. 2 of the LDNMOS and the LDPMOS at the next stage of their formation after that of Fig. 3,

Fig. 5 is a view similar to Fig. 2 of the LDNMOS and the LDPMOS at the next stage of their formation after that of Fig. 4,

Fig. 6 is a view similar to Fig. 2 of the LDNMOS and the LDPMOS at the next stage of their formation after that of Fig. 5,

Fig. 7 is a view similar to Fig. 2 of the LDNMOS and the LDPMOS at the next stage of their formation after that of Fig. 6, and

Figs. 8(a) and (b) are transverse cross-sectional elevational views of a detail of the LDNMOS and the LDPMOS at two stages of their formation.

Detailed Description of the Invention

Referring to the drawings there is illustrated an LDNMOS indicated generally by the reference numeral 1 and an LDPMOS indicated generally by the reference numeral 2 both according to the invention, and both formed on a silicon substrate, in this embodiment of the invention a P-substrate 3 by a CMOS process using a method according to the invention. An N-well 4 for the LDNMOS 1 and a P-well 5 for the LDPMOS 2 are formed in an epitaxial layer 6 using a conventional CMOS process

which will be well known to those skilled in the art. An oxide layer for forming a locos 9 of each LDNMOS 1 and LDPMOS 2 is laid down over the N-well 4 and the P-well 5 and appropriately etched to form the respective locos 9. The oxide layer which forms the locos 9, also forms a mask 10 for defining respective areas through which dopants are implanted in the N-well 4 and P-well 5 for forming a P-body region 15, and an N-body region 16, respectively in the respective N-well 4 and P-well 5 as will be described below. A gate oxide layer 12 of approximately 12nm is laid down on the respective N and P-wells 4 and 5, and respective gates 14 of the LDNMOS 1 and the LDPMOS 2 are formed over a part of the gate oxide layer 12 and over a part of the locos 9. Up to here the formation of the LDNMOS 1 and LDPMOS 2 is carried out using a conventional CMOS process.

The P-body and N-body regions 15 and 16, respectively, are next formed in the N-well 4 and the P-well 5, respectively, beneath the gates 14 by implanting appropriate dopants using the method according to the invention, which will now be described. The mask 10 forms three sides of respective areas of the gate oxide layers 12 and in turn the surface of the N-well 4 and the P-well 5 through which the dopants are to be implanted into the N-well 4 and the P-well 5 to form the P-body and the N-body regions 15 and 16, respectively. An edge 18 of the corresponding gate 14 forms the fourth side of each mask. The edge 18 is that edge of the gate 14 which is adjacent corresponding source contact regions 20 and 21 of the respective LDNMOS 1 and LDPMOS 2 which are subsequently formed.

The P-body 15 is formed by implanting the dopant, namely, boron in the N-well 4 in two steps. In the first step the dopant is directed into the N-well 4 in the direction of

the arrows A, see Fig. 8(a), at a first angle α to the surface of the gate oxide layer 12 for forming a portion 24 of the P-body 15 beneath the gate 14 and for determining the drain/source threshold voltage, see also Fig. 3. In the second step the dopant is directed at the N-well in the direction of the arrows B, see Fig. 8(b), at a second angle β for extending the P-body 15 downwardly at 25 for determining the breakdown voltage due to punchthrough through the P-body 15, see also Fig. 4. In this embodiment of the invention the first angle α is 45° and the second angle β is 83°. This is achieved by selecting the tilt angle at which the dopant is directed towards the surface of the gate oxide layer 12 in the CMOS process. The tilt angle is measured relative to an axis 26 extending perpendicularly to the general plane defined by the wafer. The dopant is directed at the first angle α by setting the tilt angle of implant at a first tilt angle θ of 45° from the perpendicular axis 26. The dopant is implanted at the second angle β by setting the tilt angle of implant at a second tilt angle Φ of 7° from the perpendicular axis 26. The direction at which the dopant is implanted at the first and second tilt angles θ and Φ is selected so that the dopant is directed towards the surface of the gate oxide layer 12 and towards the edge 18 of the gate 14 in a general source/drain direction.

The dose level of dopant implanted at the first and second tilt angles θ and Φ may be similar or different, and the energy at which the dopant is implanted at the first and second tilt angles θ and Φ may also be similar or different. The dose and energy at which the dopant is implanted at the first tilt angle θ is determined by the desired drain/source threshold voltage of the LDNMOS 1, and the dose and energy at which the dopant is implanted at the second tilt angle Φ is determined by the desired breakdown voltage of the P-body 15. The selection of the appropriate dose and

energy levels at which the dopant is to be implanted at the first and second tilt angles θ and Φ will be known to those skilled in the art.

After the dopant has been implanted to form the P-body 15 the N-body 16 is then formed in the P-well 5 of the LDPMOS 2. The N-body 16 is formed in the P-well 5 of the LDPMOS 2 using a similar method as is used for forming the P-body 15, with the exception that the dopant is phosphorous. The phosphorous dopant is initially implanted in the P-well 5 at the first angle α of 45° using the first tilt angle θ of 45° for determining the drain/source threshold voltage of the LDPMOS 2. The phosphorous dopant is then implanted in the P-well 5 at the second angle β of 83° using the second tilt angle Φ of 7° for determining the breakdown voltage of the N-body 16. As in the case of implanting the boron dopant in the N-well 4 for forming the P-body 15, the dose of phosphorous dopant and the energy with which the phosphorous dopant is implanted at the respective first and second tilt angles θ and Φ may be similar or different, and will be determined by the desired drain/source threshold voltage and the desired punchthrough breakdown voltage of the LDPMOS 2.

After the boron and phosphorous dopants have been implanted in the N-well 4 and the P-well 5, respectively, at the first and second tilt angles θ and Φ the dopants are simultaneously diffused using a conventional CMOS polycide anneal step.

The N++ source contact region 20 and an N++ drain contact region 27 are next formed in the P-body 15 and in the N-well 4, respectively, by implanting dopants Nldd and NSD into the P-body 15 through the gate oxide layer 12, and directly into the N-well 4 by the CMOS process. The P++ source contact region 21 and a P++

drain contact region 28 are formed in the N-body 16 and the P-well 5, respectively, by implanting dopants Pldd and PSD in the N-body 16 and the P-well 5, respectively. After the Nldd dopants and the Pldd dopants have been implanted the wafer is subjected to a CMOS thermal cycle for driving the dopants into the respective P and N-bodys 15 and 16 and the N and P-wells 4 and 5. The NSD and PSD implants are subsequently driven in by a further CMOS thermal cycle. The formation of N++ and P++ regions will be well known to those skilled in the art.

Thereafter, the process for forming the LDNMOS 1 and the LDPMOS 2 continues using the conventional CMOS process, and the remaining process steps will thus be well known to those skilled in the art.

Although described for forming LDMOS devices, the method according to the invention may also be used for forming vertical DMOS devices. It will of course be appreciated that although not described, CMOS devices may also be formed on the wafer either simultaneously or sequentially with the formation of the LDMOS devices. While the LDMOS devices have been described as being formed using a CMOS process, it will of course be appreciated that the LDMOS devices may be formed using a BiCMOS process, in which case, bipolar CMOS devices may also be formed simultaneously or sequentially with the DMOS devices.

While in the embodiment of the invention described the P-body region has been described as being implanted before the N-body region, it will be appreciated that the P-body and N-body regions may be formed in any order.

Claims

1. A method for forming a body region in a drain region of a DMOS device on a wafer after the gate has been formed with the body region extending partly beneath a gate of the DMOS device and appropriately aligned with the gate, the drain region defining a surface plane, the method comprising the steps of:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

2. A method as claimed in Claim 1 in which the dopant is directed at the first angle towards the surface plane in step (a) in a general source/drain direction.

3. A method as claimed in Claim 1 in which the dopant is directed at the second angle towards the surface plane in step (b) in a general source/drain direction.

4. A method as claimed in Claim 1 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 30° to 60°.

5. A method as claimed in Claim 4 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) is approximately 45°.

6. A method as claimed in Claim 1 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 70° to 90°.

7. A method as claimed in Claim 6 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) is approximately 83°.

8. A method as claimed in Claim 1 in which the dopant is implanted in the drain region in each of steps (a) and (b) using an edge of the gate adjacent the source as part of a mask for defining a portion of the surface of the drain region through which the dopant is to be implanted.

9. A method as claimed in Claim 1 in which the dopant implanted in each of steps (a) and (b) may be the same or different, and the dopant implanted in each of steps (a) and (b) may be implanted at the same or different dose and/or energy levels.

10. A method as claimed in Claim 1 in which the dopant implanted in the drain region in each of steps (a) and (b) is diffused by a dopant diffusion process for forming the body region.

11. A method as claimed in Claim 1 in which the drain region is formed by an N-well, and the body region is formed as a P-body, and the dopant of each of steps (a) and (b) is boron.

12. A method as claimed in Claim 1 in which the drain region is formed by a P-well, and the body region is an N-body, and the dopant of each of steps (a) and (b) is phosphorous.

13. A method as claimed in Claim 1 in which the dose and energy levels of the dopant implanted in each of steps (a) and (b) are sufficient for providing the desired drain/source threshold voltage and the breakdown voltage through the drain region.

14. A method as claimed in Claim 1 in which the method for forming the body region in the drain region of the DMOS device is a CMOS process.

15. A method as claimed in Claim 1 in which the DMOS device is an LDMOS device.

16. A DMOS device comprising a drain region defining a surface plane, a gate located on the drain region, and a body region formed in the drain region and

extending partly beneath the gate and appropriately aligned therewith, the body region being formed after the gate region has been formed by:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

17. A DMOS device as claimed in Claim 16 in which the dopant is directed at the first angle towards the surface plane in step (a) in a general source/drain direction.

18. A DMOS device as claimed in Claim 16 in which the dopant is directed at the second angle towards the surface plane in step (b) in a general source/drain direction.

19. A DMOS device as claimed in Claim 16 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) lies in the range of 30° to 60°.

20. A DMOS device as claimed in Claim 19 in which the first angle to the surface plane of the drain region at which the dopant is directed in step (a) is approximately 45°.

21. A DMOS device as claimed in Claim 16 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) lies in the range of 70° to 90°.

22. A DMOS device as claimed in Claim 21 in which the second angle to the surface plane of the drain region at which the dopant is directed in step (b) is approximately 83°.

23. A DMOS device as claimed in Claim 16 in which the body region in the drain region of the DMOS device is formed by a CMOS process.

24. A DMOS device as claimed in Claim 16 in which the DMOS device is an LDNMOS device.

25. A DMOS device as claimed in Claim 16 in which the DMOS device is and LDPMOS device.

26. An integrated circuit chip comprising a DMOS device as claimed in Claim 16.

27. An integrated circuit chip comprising a DMOS device formed thereon by the method of Claim 1.

ABSTRACT

"A method for forming a DMOS device and a DMOS device"

A method for forming an LDNMOS (1) and LDPMOS (2) in a CMOS process comprises forming the LDNMOS (1) and LDPMOS (2) to a stage where a gate (14) is laid down on a gate oxide layer (12) and a locos (9) is formed over the respective N and P-wells (4) and (5) of the LDNMOS (1) and LDPMOS (2). A P-body (15) is formed in the N-well (4) of the LDNMOS (1) by implanting a boron dopant in two stages, in the first stage at a first tilt angle (θ) of 45° for forming the P-body (15) beneath the gate (14) for determining the source/drain threshold voltage, and subsequently at a second tilt angle (Φ) of 7° for extending the P-body (15) downwardly at (25) for determining the punchthrough breakdown voltage of the LDNMOS (1). The formation of an N-body (16) in a P-well (5) of the LDPMOS (2) is similar to the formation of the P-body (15) with the exception that the dopant is a phosphorous dopant.

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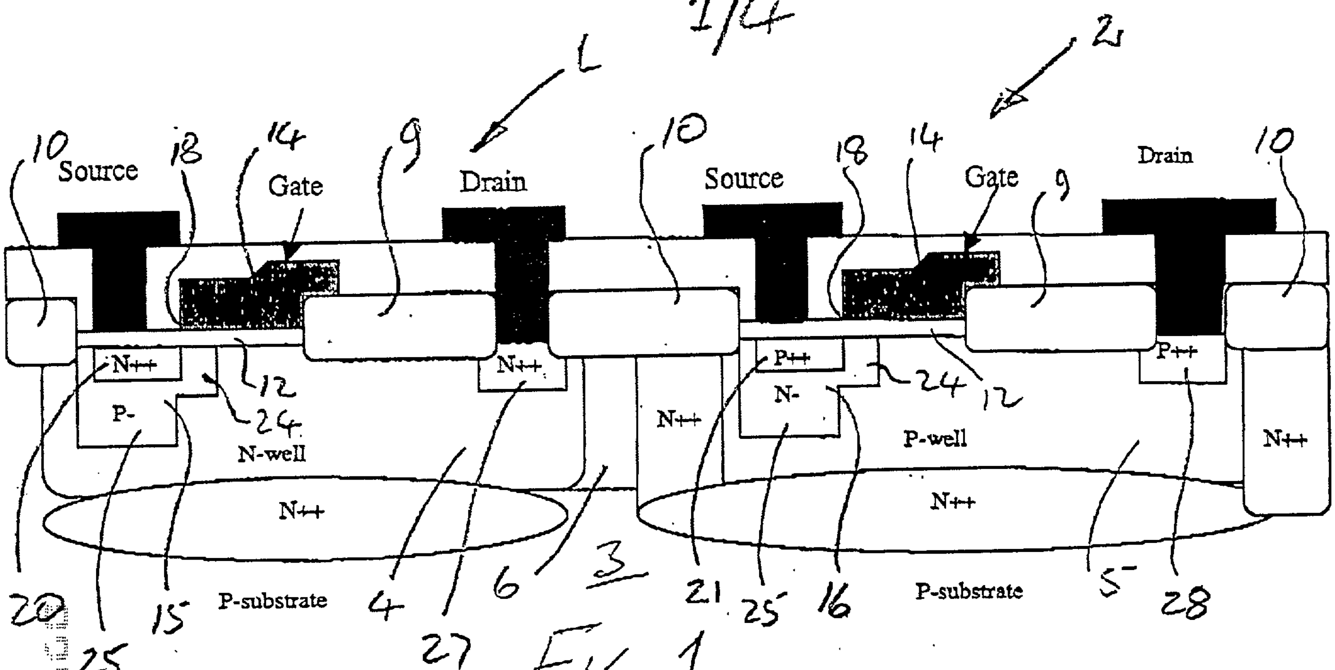


FIG 1

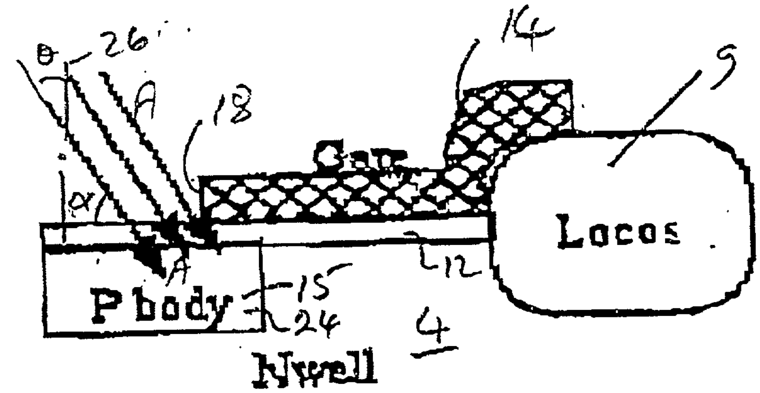


FIG 8(a)

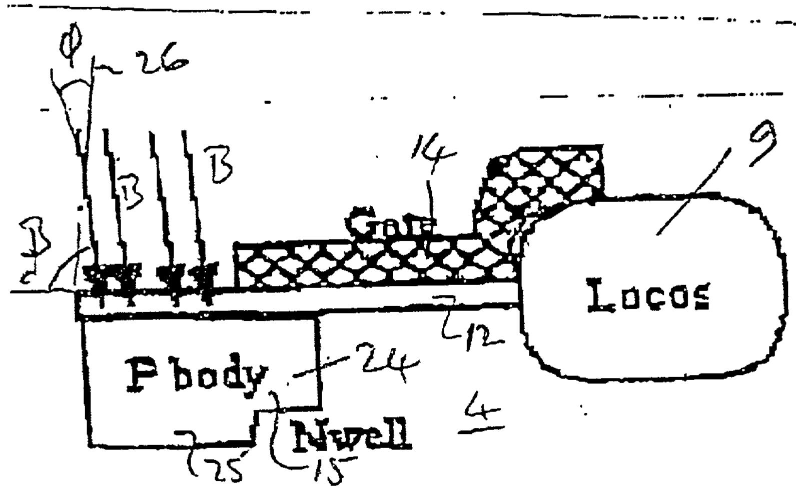


FIG 8(b)

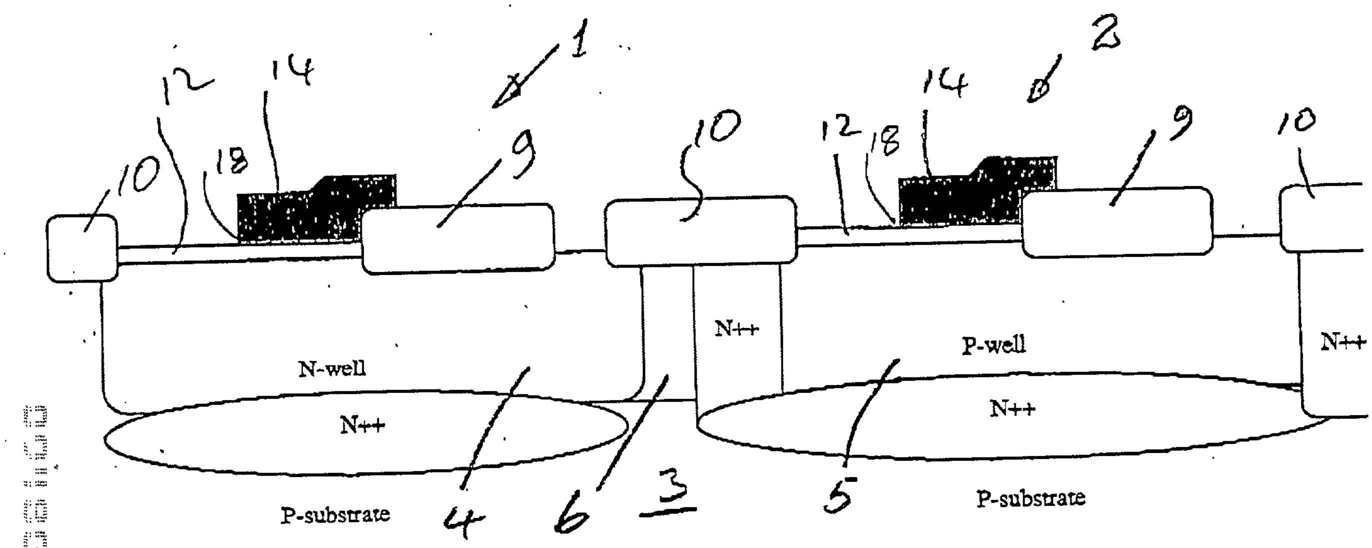
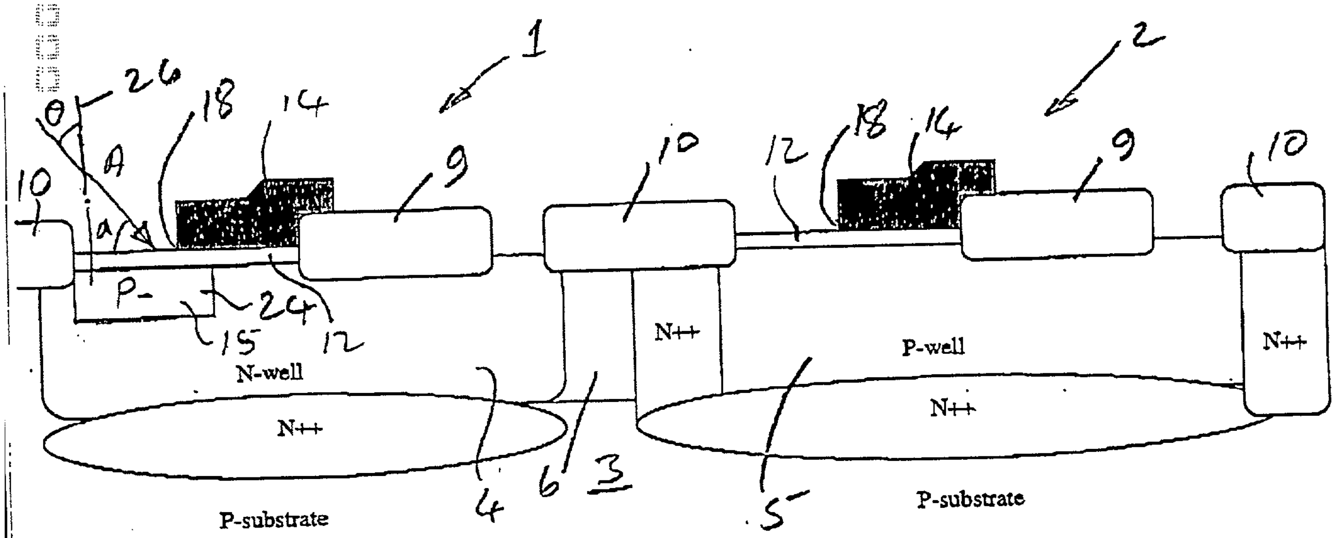


FIG 2



$\alpha = 45^{\circ}$

FIG 3

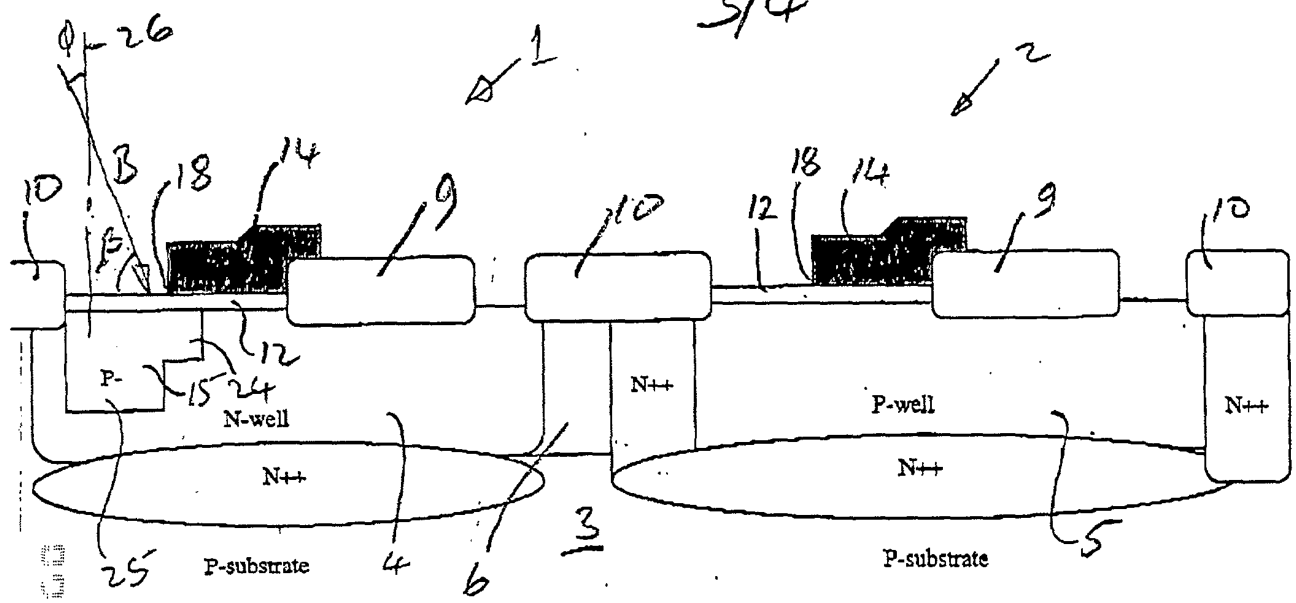

φ
26
1
2
B
β
18
14
10
9
12
P-
15
24
N-well
N++
N++
P-well
N++
25
P-substrate
4
6
3
P-substrate
5
φ = 7°

FIG 4

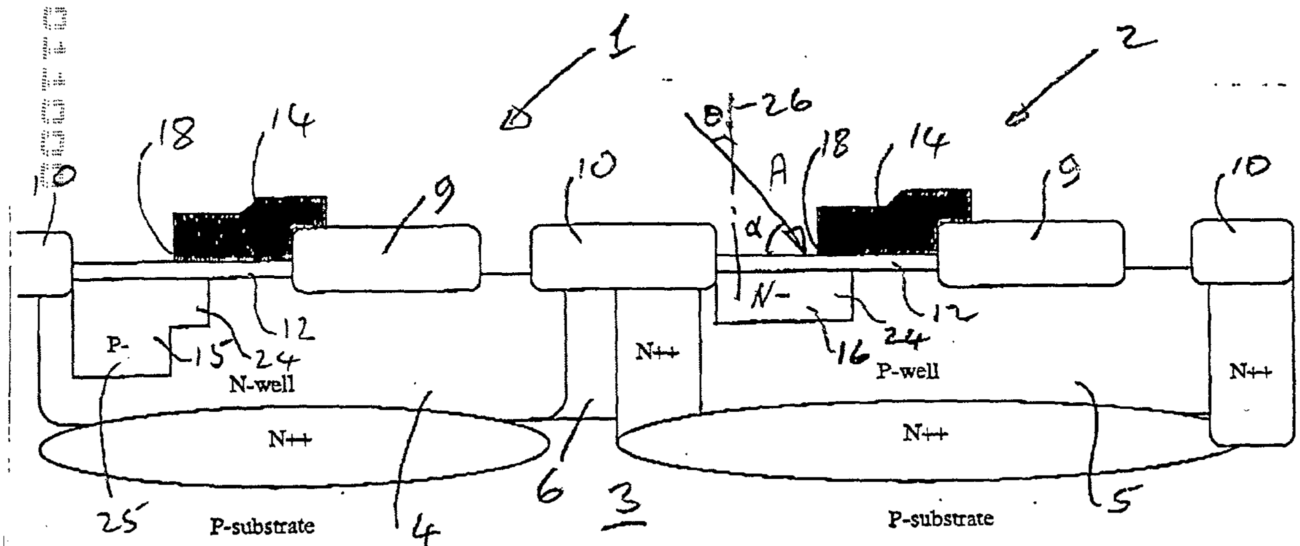

1
2
θ
26
18
14
A
10
9
α
N-
12
16
24
P-
15
N-well
N++
P-well
N++
N++
25
P-substrate
4
6
3
P-substrate
5

FIG 5

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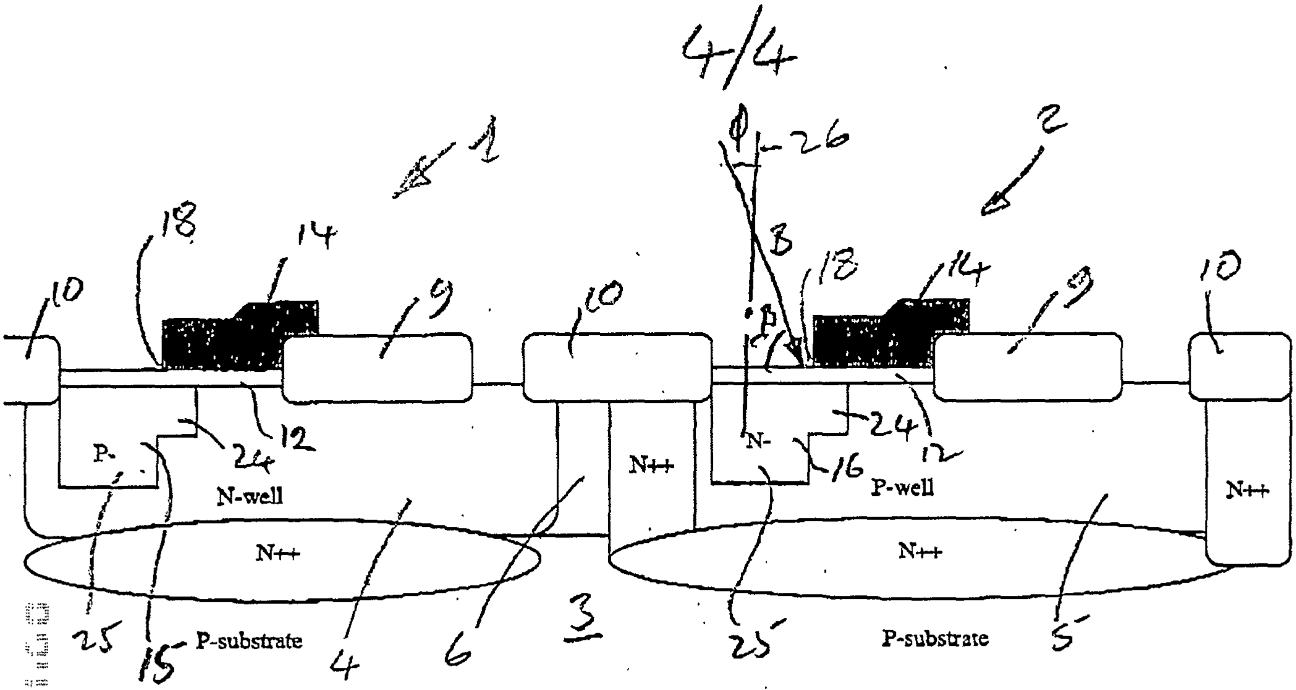
1
2
φ
26
B
P
18
14
9
10
10
9
10
P-
24
12
N-
24
12
16
N-well
P-well
N++
N++
N++
N++
25
15
P-substrate
4
6
3
25
P-substrate
5

FIG 6

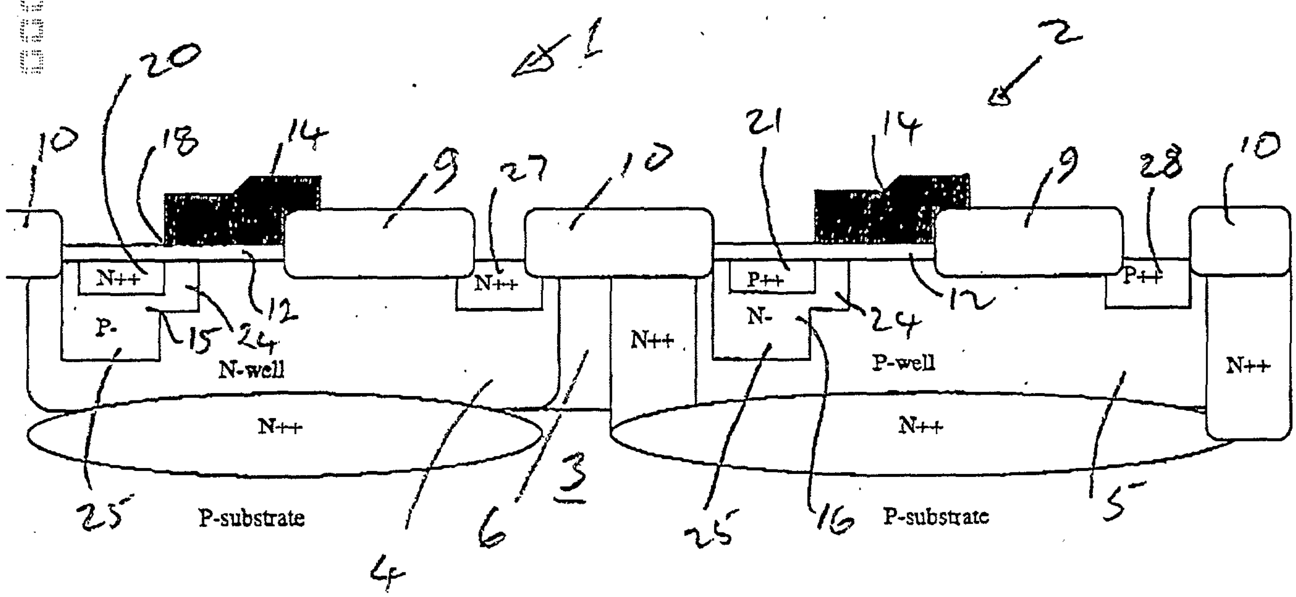
1
2
20
10
18
14
9
27
10
21
14
9
28
10
N++
N++
P++
P++
P-
15
24
12
N-
24
12
N-well
P-well
N++
N++
N++
N++
3
25
P-substrate
4
6
25
16
P-substrate
5

FIG 7

Attorney Docket No. A0418/______

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"A method for forming a DMOS device and a DMOS device"

the specification of which is attached hereto unless the following is checked:

[ ] was filed on ______________, as United States Application No. ______________ (Include Series Code) or PCT International Application No. ______________, bearing attorney docket No. ______________, and was amended on ______________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or section 365(a) of any PCT International application designating at least one country other than the United States listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign PCT International Application(s) and any priority claims under 35 U.S.C. §§119 and 365(a), (b):

			Priority Claimed	
(Number)	(Country-if PCT, so indicate)	(DD/MM/YY Filed)	[ ] YES	[ ] NO
(Number)	(Country)	(DD/MM/YY Filed)	[ ] YES	[ ] NO
(Number)	(Country)	(DD/MM/YY Filed)	[ ] YES	[ ] NO

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

(Application Number)	(filing date)
(Application Number)	(filing date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT International application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.)	(filing date)	(status-patented, pending, abandoned)
(Application No.)	(filing date)	(status-patented, pending, abandoned)

PCT International Applications designating the United States:

(PCT Appl. No.) (U.S. Ser. No.) (PCT filing date) (status-patented, pending, abandoned)

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